



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application of:

Tinku

Application No.: 09/817,711

Filed: March 26, 2001

For: TWO-DIMENSIONAL PYRAMID FILTER
ARCHITECTURE

Examiner: not yet assigned

Art Unit: not yet assigned

PRELIMINARY AMENDMENTBox Non-Fee Amendment
ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Dear Sir:

Please make the following amendment and consider the following remarks. A marked version to show the changes that have been made is attached herewith.

IN THE SPECIFICATION:

Please amend the specification by substituting the paragraph below for the last paragraph on page 11:

Equation [1] above illustrates that a direct two-dimensional pyramid filter architecture of order $2N-1$, in this case where N is three, may potentially be implemented using either four two-dimensional pyramid filters of order $[2(N-1)-1]$ or one two-dimensional pyramid filter of order $[2(N-1)-1]$ using four signal sample matrices $P_{i-1,j-1}^{3 \times 3}$, $P_{i-1,j+1}^{3 \times 3}$, $P_{i+1,j-1}^{3 \times 3}$, $P_{i+1,j+1}^{3 \times 3}$ and two one-dimensional pyramid filters of order $2N-1$, here row-wise and column-wise, in this example.

FIG. 3 is a schematic diagram illustrating such an embodiment, although, of course, the

claimed subject matter is not limited in scope to this particular implementation or embodiment. For example, the output signal samples corresponding to those produced by four two-dimensional pyramid filters of order $2(N-1)-1$, here order three where N is three, may not necessarily be produced by two-dimensional pyramid filters. As just one example, these output signals may be produced using one-dimensional pyramid filters. One such filter is shown in FIG. 2, although, again, additional approaches to producing the output signals for the architecture shown in FIG. 3 may also be employed.

REMARKS

It is respectfully requested that the Examiner enter the foregoing changes to the specification and indicate approval of FIG. 3, submitted herewith. The foregoing amendment is to correct some inadvertent typographical errors in the specification and new FIG. 3 includes reference numerals that are employed in the specification, but were inadvertently omitted from the submitted figure. No new matter is entered.

CONCLUSION

In view of the foregoing, it is respectfully requested that the Examiner enter the foregoing amendment and approve the new figure submitted. If the Examiner has any questions, he is invited to contact the undersigned at (503) 264-0967. Consideration of this patent application and early allowance of all the claims is respectfully requested.

Respectfully submitted,

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Dated:

4/25/01

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053474-053004

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Director, U.S. Patent and Trademark Office, Washington, D.C. 20231 on

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Mary Wainner
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Signature Date

MARKED VERSION TO SHOW THE CHANGES THAT HAVE BEEN MADE

Equation [1] above illustrates that a direct two-dimensional pyramid filter architecture of order $2N-1$, in this case where N is three, may potentially be implemented using either four two-dimensional pyramid filters of order $[2(N-1)-1]$ or one two-dimensional pyramid filter of order $[2(N-1)-1]$ using four signal sample matrices $P_{i-1,j-1}^{3 \times 3}$, $P_{i-1,j+1}^{3 \times 3}$, $P_{i+1,j-1}^{3 \times 3}$, $P_{i+1,j+1}^{3 \times 3}$ and two one-dimensional pyramid filters of order $2N-1$, here row-wise and column-wise, in this example.

FIG. 3 is a schematic diagram illustrating such an embodiment, although, of course, the claimed subject matter is not limited in scope to this particular implementation or embodiment. For example, the output signal samples corresponding to those produced by four two-dimensional pyramid filters of order $2(N-1)-1$, here order three~~five~~ where N is three, may not necessarily be produced by two-dimensional pyramid filters. As just one example, these output signals may be produced using one-dimensional pyramid filters. One such filter is shown in FIG. 2, although, again, additional approaches to producing the output signals for the architecture shown in FIG. 3 may also be employed.